

PICAXE VSM Tutorial Part 4

In the fourth part of our PICAXE VSM tutorial we look at how to export a Bill of Materials (BoM). We also look at how to generate a PCB netlist for use in various PCB applications.

Bill of Materials

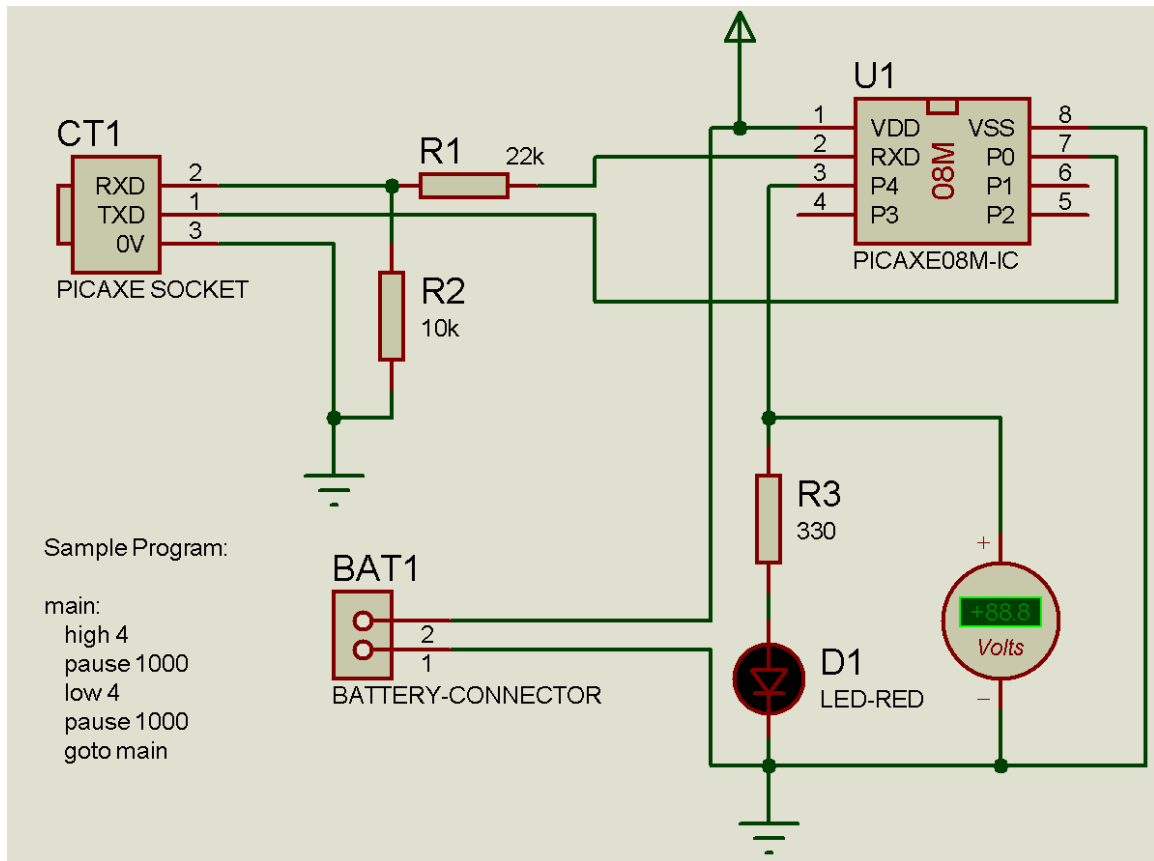


Figure 1 – simple LED circuit

Figure 1 shows the simple PICAXE-08M circuit found in the sample file 'PCB Export Demo.DSN'. We will use this file to demonstrate both a Bill of Materials and PCB netlist export.

At this point is important to note that the 'voltmeter' component must have its 'Exclude from PCB Layout' property checked. This is because you do not want it to be included in either the BoM or PCB layout.

When an export is performed, the data included within both types of export is defined as properties within each component symbol. For instance if you right click over the PICAXE-08M part and select ‘Edit Properties’ you will see the information in Figure 2.

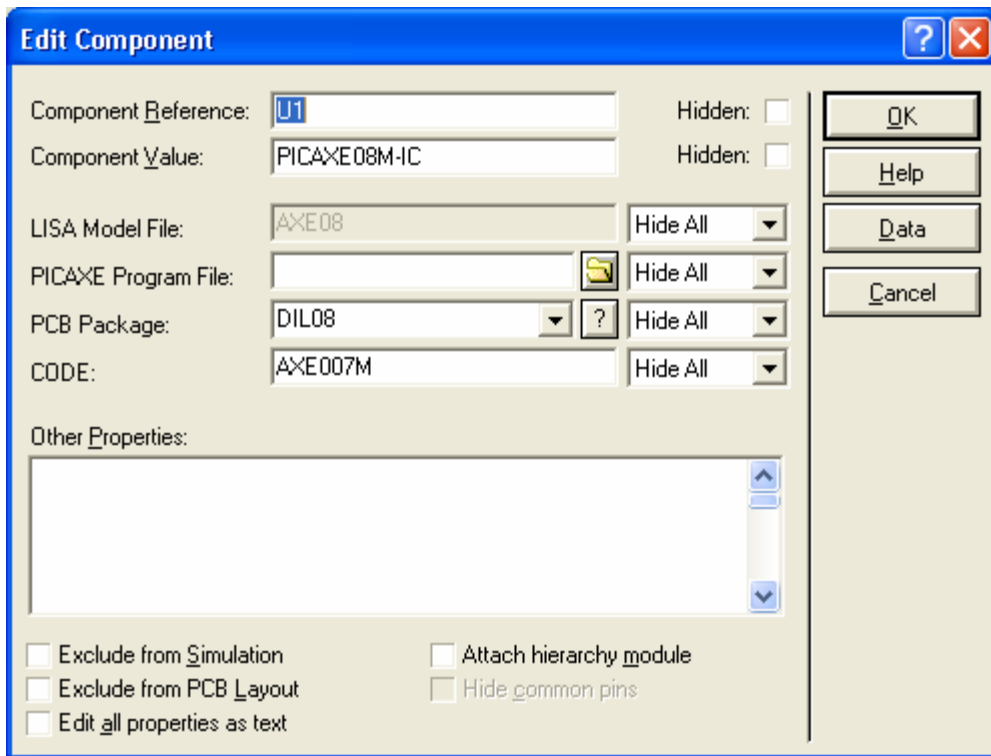


Figure 2 – PICAXE-08M properties, showing CODE and PCB Package

The ‘CODE’ property is the order code used within the Bill of Materials. By default these are set to Revolution’s online store (www.techsupplies.co.uk) order codes, but if you use a different supplier you can edit the order codes as you choose.

The ‘PCB Package’ property describes the footprint symbol used within the PCB application. We will come back to this later.

To generate the actual BoM simply click the Tools>Bill of Materials menu. You will then see an output similar to Figure 3.

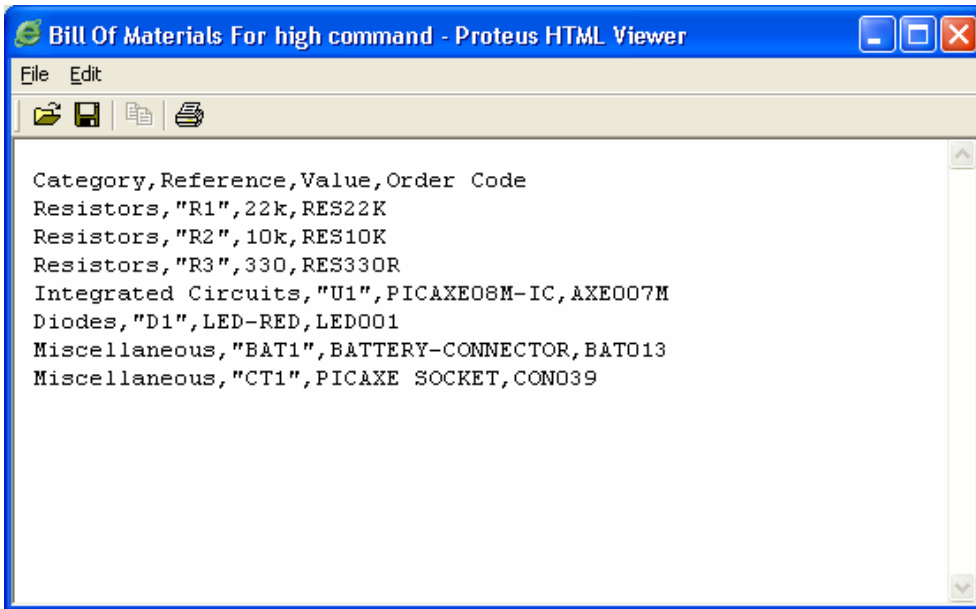


Figure 3 – Generated BoM

Once the BoM has been saved in the CSV (comma separated variables) text format it can be imported into a number of other applications e.g. Excel. Figure 4 shows the Excel layout after the file has been opened and prices added (remember to choose the Text (CSV) file format when using File>Open within Excel).

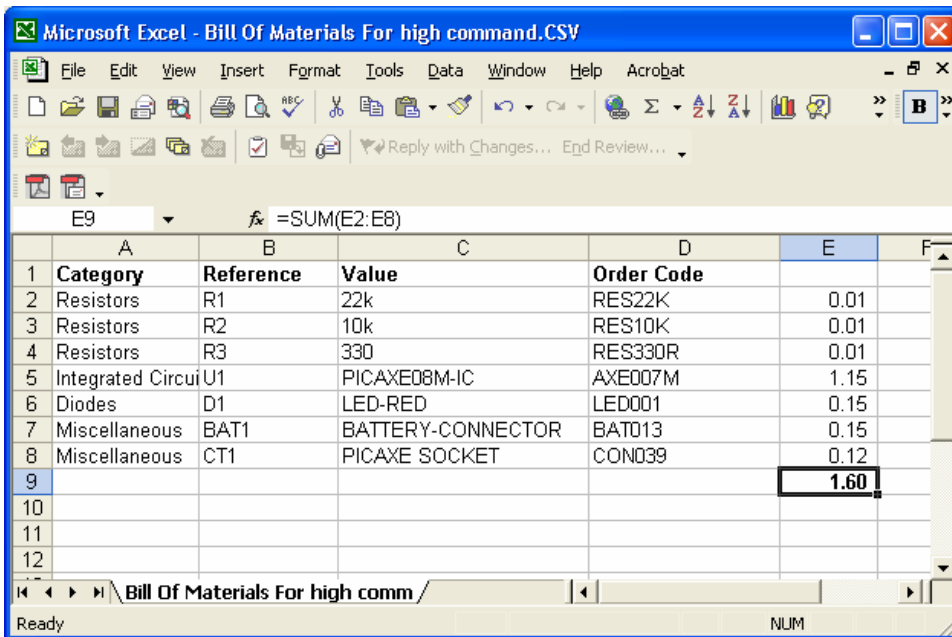


Figure 4 – Excel with prices added and totalled

PCB Netlists

PICAXE VSM does not contain a PCB layout feature, but the circuit schematics can be exported as a netlist to use in a wide variety of popular PCB applications. Over a dozen different PCB applications are supported by the netlist export option. Our recommendations would be:

Professional	- ARES from www.labcenter.com	£150 / \$US 300
Educational	- realPCB from www.techsupplies.co.uk	£50 / \$US 100
Budget	- Eagle from www.cadsoft.de	Free version

In this tutorial we will consider both the ARES and realPCB options.

Figure 1 shows a circuit suitable for generating a PCB netlist. The most important point to note is the addition of the battery connector part – after all you need somewhere to connect the power supply to your PCB! So this part has no affect on the simulation (and indeed should be excluded from the simulation) but is essential to ensure the PCB is correctly generated – otherwise there will be no pads on the PCB to connect the power supply!

To transfer to ARES or realPCB we need to create a ‘netlist file’. A netlist contains connection information about the components in the design – e.g. in our case that the LED D1 is connected to resistor R3 and 0V. For a netlist to operate correctly the components in the schematic must know the name of the corresponding footprint symbol in the PCB software – for instance that the PICAXE IC uses the 8 pin DIL IC format footprint.

This information is stored as the ‘PCB package’ property. If you right click over the PICAXE-08M symbol and select ‘Edit Properties’, you will see the PCB package name for this part is ‘DIL08’ (see Figure 2). This is actually the footprint name used by the ARES package (we will come back to how the realPCB footprint name is defined later).

Netlist Compiler

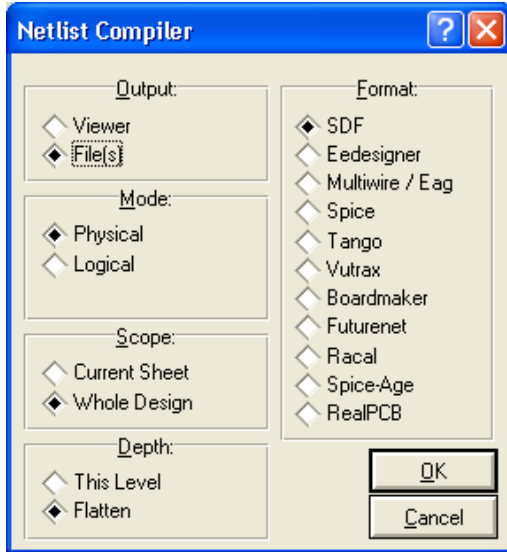



Figure 5 – Netlist export options showing PCB applications supported.

To export a netlist select the Tools>Netlist Compiler menu. The most important option is the Format as not all netlist formats are the same. So select ‘SDF’ for ARES, ‘RealPCB’ for realPCB and ‘Multiwire/Eagle’ for Eagle.

The Output option is normally used on File, to save the netlist directly to a file on your hard-drive. However if you first want to preview the netlist, select Viewer instead. This will display the contents of the netlist on-screen after it is generated – it can then be saved if desired. Depth, Scope and Mode should all be left on the defaults shown.



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ISIS NETLIST - ISIS for PICAXE VSM
FORMAT,CROCODILENETLIST,1
;Generated by ISIS for PICAXE VSM from design high command

COMPONENTFIELDS,"Value"

NET,"N001","Signal"
NET,"N003","Signal"
NET,"N004","Signal"
NET,"N005","Signal"
NET,"N006","Signal"
NET,"GND","Power"
NET,"VCC","Power"

COMPONENT,BAT1,"Battery","Connectors.cml","BATTERY-CONNECTOR"
PIN,BAT1,1,"GND"
PIN,BAT1,2,"VCC"

COMPONENT,CT1,"PICAXE Download Socket","Microcontrollers.cml","PICAXE SOCKET"
PIN,CT1,1,"N003"
PIN,CT1,2,"N004"
PIN,CT1,3,"GND"

COMPONENT,D1,"LED (white 5mm)","Light Outputs.cml","LED-RED"
PIN,D1,2,"N001"
PIN,D1,1,"GND"

COMPONENT,R1,"Resistor","Passive Components.cml","22k"
PIN,R1,1,"N004"
PIN,R1,2,"N006"

COMPONENT,R2,"Resistor","Passive Components.cml","10k"
PIN,R2,1,"N004"
PIN,R2,2,"GND"

COMPONENT,R3,"Resistor","Passive Components.cml","330"
PIN,R3,1,"N005"
PIN,R3,2,"N001"

COMPONENT,U1,"08DIL","PCB Footprints.cml","PICAXE08M-IC"
PIN,U1,1,"VCC"
PIN,U1,2,"N006"
PIN,U1,3,"N005"
PIN,U1,7,"N003"
PIN,U1,8,"GND"

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Figure 6 - sample realPCB netlist content.

Importing into ARES.

Once the netlist is generated, start up the ARES application and select File>Load Netlist. Browse to and open the .SDF netlist file. The components will all be placed in the object selector, and after manual placing will appear as in figure 7 (obviously you will probably layout differently!) The nets will be shown as lines – this is commonly known as a ‘rats-nest’ layout as the tracks are not yet drawn.

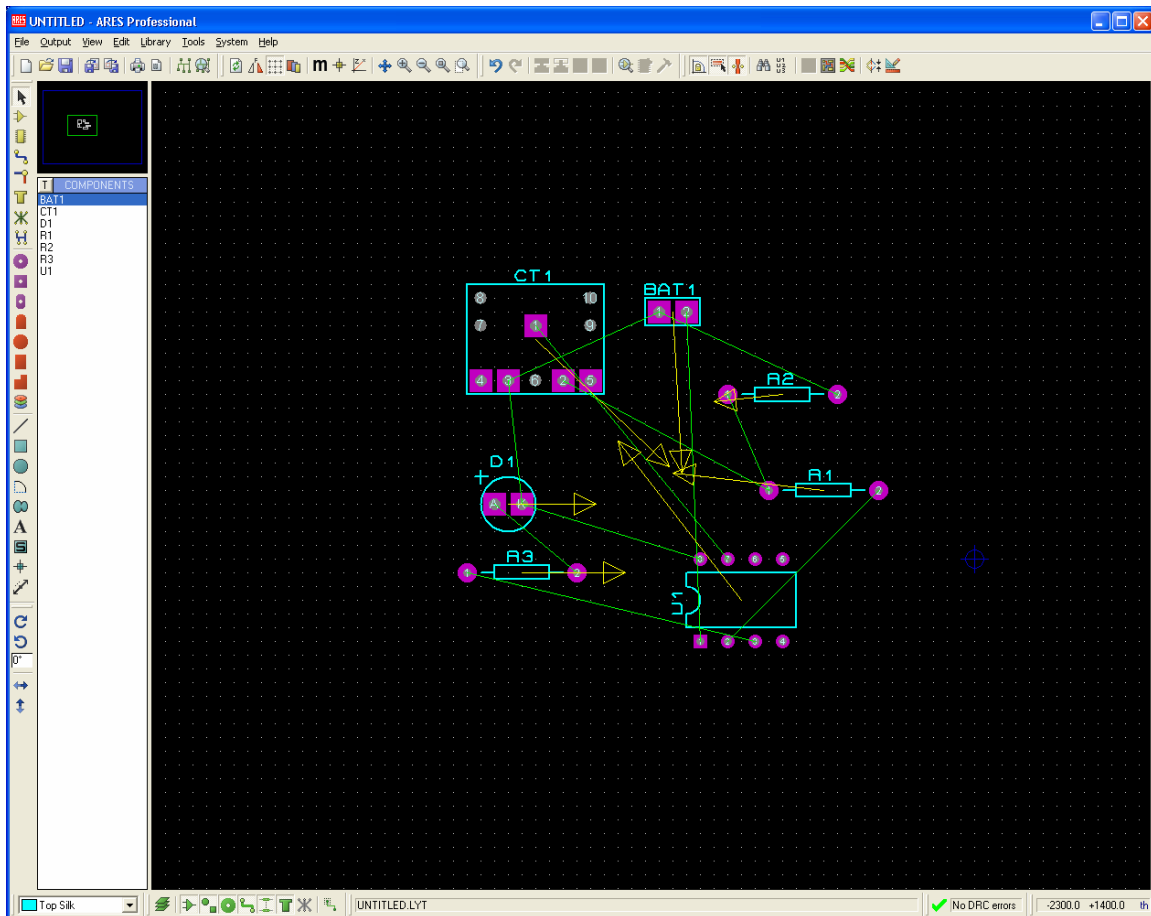


Figure 7 – ARES layout before auto-routing.

Now select Tools>Autorouter menu to change your 'rats-nest' into a proper PCB, as shown in Figure 8. Naturally this sample design could be tidied up by moving the parts closer and rearranging!

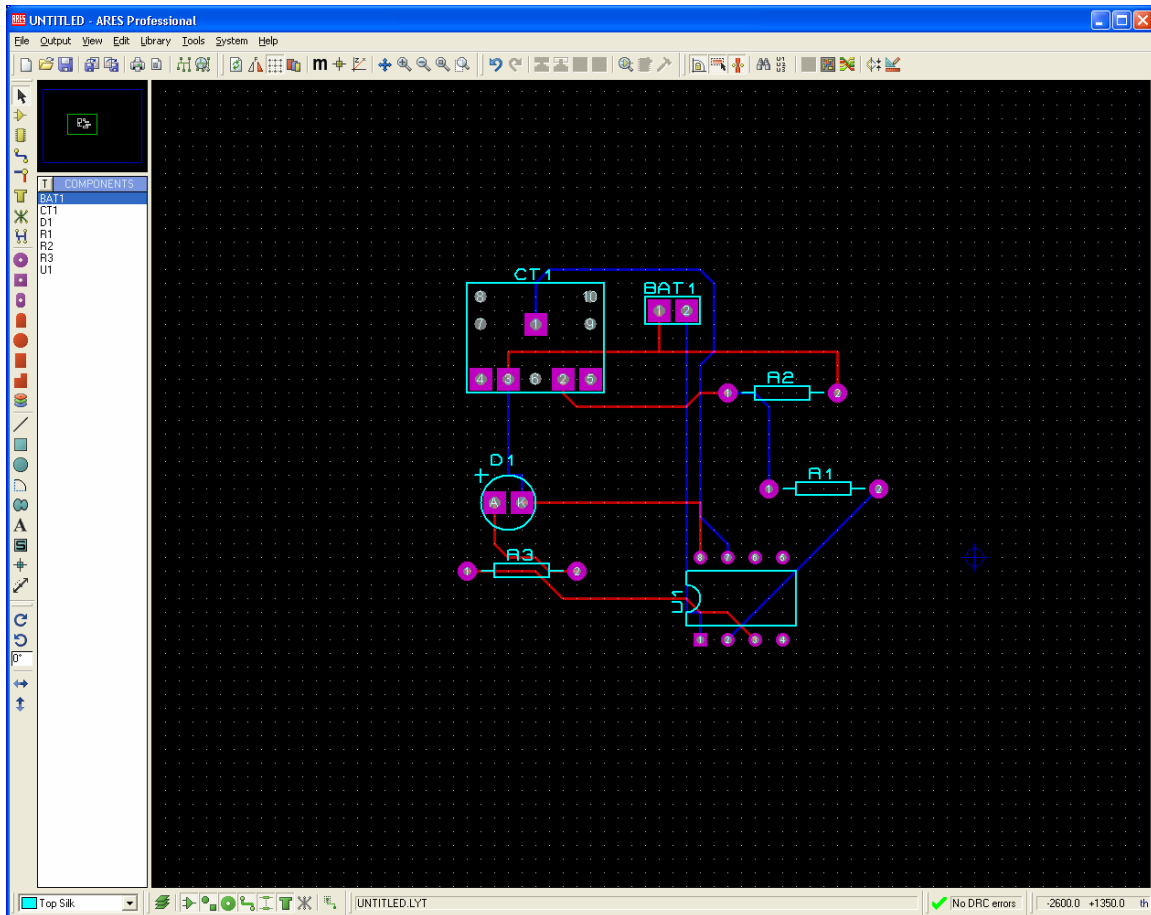


Figure 8 – ARES layout after auto-routing.

Now the design can be manually completed and used to produce manufacturing Gerber files if required.

Importing into realPCB.

Once the netlist is generated, start up the realPCB application and select the File>Import menu. Browse to and open the .CIR netlist file.

realPCB has a fully automated import so if you simply click ‘Next’ through all the import wizard stages you will end up with a PCB layout as shown in Figure 9

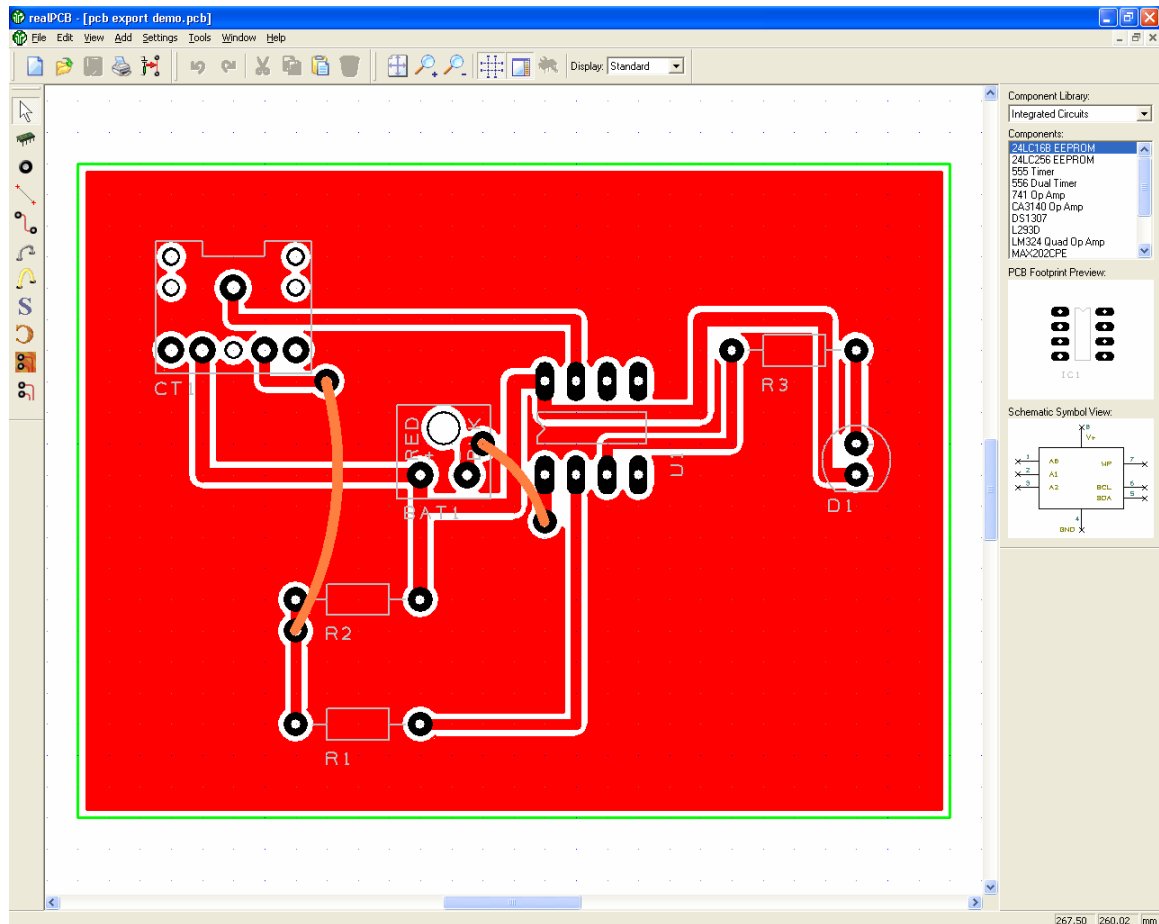


Figure 9 – realPCB layout after single sided import

Naturally you will probably want to move the components and tidy up the design manually after the import. Then the design can be manually completed and used to produce manufacturing Gerber files if required.

realPCB Mapping File

As the realPCB footprint names do not always match the ARES footprint names, a special mapping file called realPCB.adi is found in the PICAXE VSM\LIBRARY folder. This file defines how the ‘PCB Package’ (ARES footprint) property is translated to a realPCB footprint name upon the realPCB netlist export. If required this file can be edited by the end user to add additional translations or modify existing translations.

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REALPCB.ADI - Notepad
File Edit Format View Help
; This file describes rules for package and pin translation from Proteus to realPCB
; All packages within ISIS are in Proteus ARES format
; This file translates to best suitable part in realPCB
; You can swap pins over via the fourth column, "proteus_pin_name = realpcb_pin_name"

DATA PACKAGE      : REALPCB_LIBRARY, REALPCB_PACKAGE, REALPCB_PINS

CONN-SIL2         : "Connectors.cml", "Header (2 pole)",      [SKIP]
CONN-SIL3         : "Connectors.cml", "Header (3 pole)",      [SKIP]
CONN-SIL4         : "Connectors.cml", "Header (4 pole)",      [SKIP]
CONN-SIL5         : "Connectors.cml", "Header (5 pole)",      [SKIP]
CONN-SIL6         : "PCB Footprints.cml", "06SIL",           [SKIP]
CONN-SIL8         : "PCB Footprints.cml", "08SIL",           [SKIP]
CONN-SIL9         : "PCB Footprints.cml", "09SIL",           [SKIP]
CONN-SIL10        : "Connectors.cml", "Header (10 pole)",     [SKIP]
DIL04             : "PCB Footprints.cml", "04DIL",           [SKIP]
DIL06             : "PCB Footprints.cml", "06DIL",           [SKIP]
DIL08             : "PCB Footprints.cml", "08DIL",           [SKIP]
DIL14             : "PCB Footprints.cml", "14DIL",           [SKIP]
DIL16             : "PCB Footprints.cml", "16DIL",           [SKIP]
DIL18             : "PCB Footprints.cml", "18DIL",           [SKIP]
DIL20             : "PCB Footprints.cml", "20DIL",           [SKIP]
DIL22             : "PCB Footprints.cml", "22DIL",           [SKIP]
DIL24             : "PCB Footprints.cml", "24DIL (wide)",     [SKIP]
DIL24NAR         : "PCB Footprints.cml", "24DIL (narrow)",   [SKIP]
DIL28             : "PCB Footprints.cml", "28DIL (wide)",     [SKIP]
DIL28NAR         : "PCB Footprints.cml", "28DIL (narrow)",   [SKIP]
DIL40             : "PCB Footprints.cml", "40DIL",           [SKIP]
DIL64             : "PCB Footprints.cml", "64DIL",           [SKIP]
LED               : "Light outputs.cml", "LED (white 5mm)",   "A=2, K=1"
LDR               : "Input Components.cml", "LDR (miniature)", [SKIP]
TO3               : "PCB Footprints.cml", "TO3",             [SKIP]
TO18              : "PCB Footprints.cml", "TO18",            [SKIP]
TO39              : "PCB Footprints.cml", "TO39",            [SKIP]
TO92              : "PCB Footprints.cml", "TO92",            [SKIP]
ELINE             : "PCB Footprints.cml", "TO92",            "1=3, 2=2, 3=1"
TO92-2           : "PCB Footprints.cml", "TO92A",           [SKIP]
TO92-100         : "PCB Footprints.cml", "TO92",            [SKIP]
TO220             : "PCB Footprints.cml", "TO220",          [SKIP]
P1               : "PCB Footprints.cml", "TO220",          [SKIP]
RES40             : "Passive Components.cml", "Resistor",     [SKIP]
DIODE25          : "Discrete Semiconductors.cml", "1N4148 Diode", "A=1, K=2"
DIODE30          : "Discrete Semiconductors.cml", "1N4001 Diode", "A=1, K=2"
DIODE40          : "Discrete Semiconductors.cml", "1N4001 Diode", "A=1, K=2"
D035             : "Discrete Semiconductors.cml", "1N4001 Diode", "A=1, K=2"
D035             : "Discrete Semiconductors.cml", "1N4148 Diode", "A=1, K=2"
D041             : "Discrete Semiconductors.cml", "Zener Diode", "A=1, K=2"
CONN-DIL14       : "PCB Footprints.cml", "14DIL",           [SKIP]
7SEG-56         : "Light outputs.cml", "7 Seg LED(CA)",
" E1=1, D1=2, CA1=3, C1=4, DP1=5, B1=6, A1=7, F1=9, G1=10"
PICAXE-SOCKET    : "Microcontrollers.cml", "PICAXE Download Socket", [SKIP]
RESONATOR        : "Microcontrollers.cml", "Resonator",      [SKIP]

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Figure 10 – realPCB mapping file